

## IN THE CLAIMS

Claims 11-15 are pending in this application as follows:

1-10. (Canceled)

11. (Previously Presented) A liquid crystal display device comprising:

- a liquid crystal display panel;

- a first liquid crystal drive circuit and a second liquid crystal drive circuit;

- a first image signal line and a first clock signal line formed on the liquid crystal display panel, and connected with the first liquid crystal drive circuit; and

- a second image signal line and a second clock signal line formed on the liquid crystal display panel, and connected with the first liquid crystal drive circuit and the second liquid crystal drive circuit,

- wherein the first liquid crystal drive circuit comprises a first image signal input terminal connected with the first image signal line, and a first clock input terminal connected with the first clock signal line, and the second liquid crystal drive circuit comprises a second image signal input terminal connected with the second image signal line and a second clock input terminal connected with the second clock signal line;

- wherein the first liquid crystal drive circuit comprises a compensation circuit configured to generate an internal clock signal based on a clock received from the first clock input terminal signal compensating for a duty ratio deviation of the received clock signal, the internal clock signal swinging from a first voltage to a second voltage lower than the first voltage,

- a data select circuit configured to select digital image data received from the first image signal input terminal at a timing of a voltage change from the first voltage to the second voltage as a first digital image data and at a timing of a voltage change from the second voltage to the first voltage of the internal clock signal as a second digital image data;

- a first data bus configured to transmit the first digital image data from the data select circuit,

- a second data bus configured to transmit the second digital image data from the data select circuit,

a select voltage circuit configured to select a voltage according with the first and the second digital image data to drive the liquid display panel,

a image signal output circuit configured to output the digital image data received from the first image signal input terminal to the second liquid crystal drive circuit via the second image signal line, and

a clock signal output circuit configured to delay the internal clock signal and output the delayed clock signal to the second liquid crystal drive circuit via the second clock signal line.

12. (Previously Presented) The liquid crystal display device as claimed in claim 11, wherein the image signal output circuit configured to output the digital image data transmitted on the first data bus and the second data bus.
13. (Previously Presented) The liquid crystal display device as claimed in claim 11, wherein the clock signal output circuit configured to delay the internal clock signal provides phase margins thereof in a dual-edge accept scheme.
14. (Previously Presented) The liquid crystal display device as claimed in claim 13, wherein the clock compensation circuit comprises a phase locked loop circuit.
15. (Previously Presented) The liquid crystal display device as claimed in claim 13, wherein the clock compensation circuit comprises a delay locked loop circuit.